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STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER
AUDUONG, GENE NGHIA

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/020,208	Applicant(s) BHATTACHARYA ET AL.	
	Examiner Gene N Auduong	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. This office acknowledges receipt of the following items from the applicant:

- Information Disclosure Statement (IDS), filed on April 8, 2003.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Mo et al. (U.S. Pat. No. 5,956,279).

Regarding claim 13, Mo et al. disclose a Static Random access memory device comprising: a test circuit (precharge circuit 200 conjunction with the burn-in current source circuit 300) integrated with the SRAM array; and connections that couple the test circuit to the SRAM array; wherein during probing (during wafer burn-in testing), the test circuit (precharge circuit 200 conjunction with the burn-in current source circuit 300) applies a voltage difference across a plurality of adjacent bitline pairs and/or wordline pairs of the SRAM array (col. 2, lines 8-26, col. 3, line 64 – col. 4, line 30; col. 5, lines 15-39); the voltage being larger than an operational supply voltage for the SRAM array (col. 1, lines 49-53), to thereby induce failure of metal stringers or defects (col. 1, lines 25-53; col. 2, lines 5-25; col. 3, line 64 – col. 4, line 29; also see the description for figure 4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo et al. (U.S. Pat. 5,959,279).

Regarding claim 1, Mo et al. disclose a Static Random access memory device having a method for testing a semiconductor wafer, the semiconductor wafer having a plurality of die, comprising the steps of: (b) applying a voltage difference across a plurality of adjacent bitline pairs **and/OR** wordline pairs of one **OR** more static random access memory (SRAM) arrays of at least one die of the semiconductor wafer, the voltage being larger than an operational supply voltage for the one **OR** more SRAM arrays, to thereby induce failure of metal stringers **OR** defects (precharge circuit 200 conjunction with the burn-in current source circuit 300 response to control signals to supply the test voltage to the device; col. 1, lines 25-53; col. 2, lines 5-25; col. 3 line 64 – col. 4, line30; col. 5, lines 15-39). Mo et al. do not specifically disclose the step (a) coupling an array of probes to the semiconductor wafer.

However, for wafer burn-in testing, it's known and obvious to one skill in the art that the memory device under test, must be probing to the test device in order to establish the communication between the test device and the device under test so that the test signals can supply to the device and the test result can send back to the tester to determine the condition of the device under test. Therefore, it would have been obvious to one of ordinary skill in the art at

the time the invention was made to modify Mo's device to include the limitation of the method to include the step (a) coupling an array of probes to the semiconductor wafer as a first step to establish the communication between the test device and the device under test prior the step supplying the test signals to the device and the test result can send back to the tester to determine the condition of the device under test.

Regarding claim 2, Mo et al. disclose all of the method steps of claim 1, further comprising the step of simultaneously applying the voltage across respective pairs of substantially all parallel bitline pairs **AND/OR** wordlines pairs of the one **OR** more SRAM arrays (col. 2, lines 54-61, col. 3, lines 20-31; col. 4, lines 22+).

Regarding claim 3, Mo et al. disclose all of the method steps of claim 1, further comprising the step of simultaneously applying a voltage across respective pairs of substantially all parallel bitline pairs **AND/OR** wordlines pairs of the one **OR** more SRAM arrays of more that one die of the semiconductor wafer (col. 2, lines 64-61, col. 3, lines 20-31; col. 4, lines 22+).

Regarding claim 4. Mo et al. disclose all of the method steps of claim 1, further comprising the step of applying the voltage across other adjacent, parallel metal lines (metal lines can be word-lines or bit-lines) of the one **OR** more SRAM arrays (col. 2, lines 54-61, col. 3, lines 20-31; col. 4, lines 22+).

Regarding claim 5, as best understood, Mo et al. disclose all of the method steps of claim 1 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage. However, the voltage, which is being supplied to the word-lines **AND/OR** bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the

maximum allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation of the method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure.

Regarding claim 6, as best understood, Mo et al. disclose all of the method steps of claim 2 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage. However, the voltage, which is being supplied to the word-lines **AND/OR** bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation of the method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure.

Regarding claim 7, Mo et al. disclose all of the method steps of claim 3 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage. However, the voltage, which is being supplied to the word-lines **AND/OR** bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the maximum

allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation the of method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure.

Regarding claim 8, Mo et al. disclose all of the method steps of claim 4 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage. However, the voltage, which is being supplied to the word-lines **AND/OR** bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation of the method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure.

6. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo et al. (U.S. Pat. No. 5,956,279) in view of McClure (U.S. Pat. No. 5,619,462).

Regarding claim 9, Mo et al. disclose all of the method steps of claim 1 except for the step of preforming step b at an elevated temperature.

McClure discloses a circuit and method for fault detection for entire wafer stress test comprising the teaching placing the device under test into burn-in oven, elevating the device temperature and then applying the test voltage to the device to exercising the test so that the test time can be shorten and avoiding consequent burn-in of package (col. 1, lines 22-25; col. 2, lines 35-48). Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to include McClure's teaching into Mo's device to further disclose the limitation preforming step b at an elevated temperature so that the test time can be shorten and avoiding consequent burn-in of package.

Regarding claim 10, Mo et al. disclose all of the method steps of claim 9 except for the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage. However, the voltage, which is being supplied to the word-lines **AND/OR** bit-lines (metal lines) of the device under test, is equal to the operation voltage or greater than two times the operation voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure. Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to further disclose the limitation of the method to further comprising the step of applying the voltage at a magnitude of equal to **OR** greater than [two times] the operational supply voltage or at any voltage range based on the maximum allowance safe operating voltage range of the components in the device prior to failure.

Regarding claim 11, Mo et al. disclose all of the method steps of claim 3 except for the step of preforming step b at an elevated temperature.

McClure discloses a circuit and method for fault detection for entire wafer stress test comprising the teaching placing the device under test into burn-in oven, elevating the device temperature and then applying the test voltage to the device to exercising the test so that the test time can be shorten and avoiding consequent burn-in of package (col. 1, lines 22-25; col. 2, lines 35-48). Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to include McClure's teaching into Mo's device to further disclose the limitation preforming step b at an elevated temperature so that the test time can be shorten and avoiding consequent burn-in of package.

Regarding claim 12, Mo et al. disclose all of the method steps of claim 4 except for the step of preforming step b at an elevated temperature.

McClure discloses a circuit and method for fault detection for entire wafer stress test comprising the teaching placing the device under test into burn-in oven, elevating the device temperature and then applying the test voltage to the device to exercising the test so that the test time can be shorten and avoiding consequent burn-in of package (col. 1, lines 22-25; col. 2, lines 35-48). Therefore, it would obvious to one ordinary skill in the art at the time the invention was made to include McClure's teaching into Mo's device to further disclose the limitation preforming step b at an elevated temperature so that the test time can be shorten and avoiding consequent burn-in of package.

Response to Arguments

7. Applicant's arguments filed March 20, 2003 have been fully considered but they are not persuasive.

In re pages 6-9, Applicants argue that " the Mo patent discloses a testing circuit to cycle memory cells by providing a current to word or bit lines connected to the memory cells. The Mo patent discloses a testing circuit that provides sufficient current to drive multiple word or bit lines to exercise memory cells. The Mo patent does not disclose that different voltages are applied across adjacent word or bit lines. Nor does the Mo patent disclose that voltages across adjacent word or bit lines will be greater than typical operational level. Applicants further argue that "the Mo patent does not indicates that currents on the bit and word lines under test would vary, thus suggesting that the voltages across adjacent bit and word lines would – by design – be approximately equal."

In response, as set forth in previous office action (paper #2), Mo discloses a static random access memory device with burn-in test circuit comprising: a test circuit (precharge circuit 200 conjunction with the burn-in current source circuit 300) integrated with the SRAM array; and connections that couple the test circuit to the SRAM array; wherein during probing (during wafer burn-in testing), the test circuit (precharge circuit 200 conjunction with the burn-in current source circuit 300) applies a voltage difference across a plurality of adjacent bitline pairs and/or wordline pairs of the SRAM array (during testing, the test circuit charging the BL and /BL pairs in a complementary states - different voltages - by the bit line precharge circuit 200; see col. 2, lines 8-26, col. 3, line 64 – col. 4, line 30; col. 5, lines 15-39;); the voltage being larger than an operational supply voltage for the SRAM array (in order to detect defects or strength of memory cells stored in the same device, a plurality of word lines are selected at a time and an exterior voltage higher than the supply voltage is applied to each of the selected memory cells; col. 1, lines 49-53), to thereby induce failure of metal stringers or defects (col. 1,

lines 25-53; col. 2, lines 5-25; col. 3, line 64 – col. 4, line 29; also see the description for Fig. 4). Therefore, Mo patent is clearly teaching the testing circuit as claimed.

In re pages 8-9, Applicants argue that "Dependent claims 2-8 and 9-12 are patentable at least based on their dependency and for the reason discussed in claim 1".

In response, the examiner considers that claims 2-8 and 9-12, as claimed, still does not distinguish over Mo patent, Mo in view of Mclure for claims 9-12. Mo patent discloses all of the limitation in claim 1 as stated above in view of Mclure for the elevated temperature to speed up the testing cycle. Therefore, Mo patent is clearly anticipated to independent claim 1 and its dependent claims 2-8 and in view of Mclure to anticipate the step of elevated temperature.

It is noted that the features upon which applicant relies (i.e., currents on the bit and word lines under test would vary) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
May 19, 2003

David Nelms
Supervisory Patent Examiner
Technology Center 2800